

FORM PTO-1449 (REV.7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. 500426.02	APPLICATION NO. Not yet assigned
INFORMATION DISCLOSURE STATEMENT <i>(Use several sheets if necessary)</i>		APPLICANT(S) Brent Keeth		09/964,113	
		FILING DATE Concurrently herewith		GROUP ART UNIT Not yet assigned 2818	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
VP	BA	0 283 906 A1	9/28/88	EP				X
VP	BB	0 828 252 A2	3/11/98	EP			X	
VP	BC	0 840 328 A2	5/6/98	EP			X	

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

VP	BD	Descriptive literature entitled, "400MHz SDRAM, 4Mx16 SDRAM Pipelined, Eight Bank, 2.5 V Operation," SDRAM Consortium Advance Sheet, published throughout the United States, pp. 1-22
VP	BE	"Draft Standards for a High-Speed Memory Interface (SyncLink)," Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society, Copyright 1996 by the Institute of Electrical and Electronics Engineers, Inc., New York, NY, pp. 1-55.
VP	BF	Ishibashi, K. et al., "A 6-ns 4-Mb CMOS SRAM with Offset-Voltage-Insensitive Current Sense Amplifiers," IEEE Journal of Solid-State Circuits, Vol. 30, No. 4, April 1995, pp. 480-486.
VP	BG	Kuroda, T. et al., "Automated Bias Control (ABC) Circuit for High-Performance VLSI's," IEEE Journal of Solid-State Circuits, Vol. 27, No. 4, April 1992, pp. 641-648.
VP	BH	Nagai, T. et al., "A 17-ns 4-Mb CMOS DRAM," IEEE Journal of Solid-State Circuits, Vol. 26, No. 11, November 1991, pp. 1538-1543
VP	BI	Taguchi, M. et al., "A 40-ns 64-Mb DRAM with 64-b Parallel Data Bus Architecture," IEEE Journal of Solid-State Circuits, Vol. 26, No. 11, November 1991, pp. 1493-1497
VP	BJ	Taguchi M. et al., "A 40ns 64Mb DRAM with Current-Sensing Data-Bus Amplifier," ISSCC Digest of Technical Papers, 1991, TAM 6.5.
	BK	VIET Q. NGUYEN PRIMARY EXAMINER
	BL	

EXAMINER	DATE CONSIDERED
V. Nguyen	7/23/09

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

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		FILING DATE Concurrently herewith			

J1033 U.S. PTO
09/964113
09/25/01

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
VN	AA	4,991,139	2/5/91	Takahashi et al.	365	201	
VN	AB	5,029,330	7/2/91	Kajigaya	365	201	
VN	AC	5,179,537	1/12/93	Matsumoto	365	201	
	AD	5,268,639	12/7/93	Gasbarro et al.	324	158 R	
	AE	5,289,415	2/22/94	DiMarco et al.	365	190	
	AF	5,305,272	4/19/94	Matsuo et al.	365	208	
	AG	5,451,898	9/19/95	Johnson	327	563	
	AH	5,488,321	1/30/96	Johnson	327	66	
	AI	5,519,661	5/21/96	Miura	VIET Q. NGUYEN EXAMINER	365	205
	AJ	5,621,340	4/15/97	Lee et al.	327	65	
	AK	5,684,750	11/4/97	Kondoh et al.	365	205	
	AL	5,708,607	1/13/98	Lee et al.	365	189.05	
	AM	5,809,038	9/15/98	Martin	371	21.2	
	AN	5,923,594	7/13/99	Voshell	365	189.05	
	AO	5,935,263	08/10/99	Keeth et al.	714	718	
	AP	5,953,266	9/14/99	Shore	365	200	
	AQ	5,959,921	09/28/99	Manning et al.	365	208	
	AR	6,005,816	12/21/99	Manning et al.	VIET Q. NGUYEN PRIMARY EXAMINER	365	208
	AS	6,032,274	02/29/00	Manning	VIET Q. NGUYEN PRIMARY EXAMINER	718	
	AT	6,043,562	3/28/00	Keeth	257	776	
↓	AU	6,055,654	04/25/00	Martin	714	719	
VN	AV	6,067,651	5/23/00	Rohrbaugh et al.	714	738	
VN	AW	6,079,037	6/20/00	Beffa et al.	714	720	
VN	AY						

EXAMINER

V. Nguyen

DATE CONSIDERED

7/23/04

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